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Patent

Customer No.: 31561
Docket No.: 13154-US-PA
Application No.: 10/710,931

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Applicant	: Steven Sang
Application No.	: 10/710,931
Filed	: 2004/8/13
For	: METAL OXIDE SEMICONDUCTOR DEVICE FOR ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT
Art Unit	: 2815
Examiner	: WILSON, ALLAN R.

TRANSMITTAL LETTER
002-1-571-273-8300
(Via fax : 1+5 pages)

Assistant Commissioner for Patents
Alexandria, VA 22314

Dear Sir,

In response to the Office Action dated July 26, 2005(Paper No.: 0705), please find the Response to Office Action, in 5 pages.

I believe that no fee is incurred. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.: 13154-US-PA).

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date : Oct 21, 2005

By : Belinda Lee
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Docket No.: 13154-US-PA
Application No.: 10/710,931

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: WILSON, ALLAN R.

Group Art Unit: 2815

In re PATENT APPLICATION of
Applicants : Steven Sang

Serial No. : 10/710,931

Filed : August 13, 2004

For : METAL OXIDE SEMICONDUCTOR DEVICE FOR ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT

AMENDMENT

Attorney Docket: 13154-US-PA

No fee is believed to be due. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.: 13154-US-PA)

AMENDMENT AND RESPONSE TO OFFICE ACTION

United States Patent and Trademark Office
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Randolph Building
401 Dulany Street
Alexandria, VA 22314

Dear Sir,

The Office Action dated July 26, 2005, has been carefully considered. In response thereto, please consider the following remarks.

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REMARKS

Present Status of the Application

The Office Action rejected present pending claims 1-13. Specifically, the Office Action claims 1, 3-6, and 8-13 under 35 U.S.C. 102(b) as being anticipated by Yamagata (U. S. Patent 5,158,899). The Office Action rejected claims 1-3, 5-8, 10 and 11 under 35 U.S.C. 102(b) as being anticipated by Steinhoff et al. (U. S. Patent 6,424,013; hereinafter Steinhoff). Claims 1-13 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 102

The Office Action rejected claims 1, 3-6, and 8-13 under 35 U.S.C. 102(b) as being anticipated by Yamagata. The Office Action rejected claims 1-3, 5-8, 10 and 11 under 35 U.S.C. 102(b) as being anticipated by Steinhoff. Applicant respectively traverses the rejections for at least the reason set for the below.

1. In the present invention, independent claims 1 and 6, as for example shown in FIG. 2 and FIG. 3, has recited the features to create the first BJT 216 (316, 318) and the second BJT 218 (320), under the circuit connection. The drain region, as recited in claims 1 and 6, is a common drain for the two parasitic BJT's.

In addition, the extended doped region 208 adjacent between the source region 204a and the doped layer 206. These extended doped region 208, source region 204a and doped layer 206 are in the same conductive type, such as N-type in FIG. 2. In other words, the voltage level is

the same for these three regions 240a, 208, and 206. ***Particularly, the source regions 240a and the doped layer 206 are at the same common voltage level.***

Further, under the semiconductor structure of the present invention, the twp parasitic BJT's 216 and 218 can be obtained with the specific circuit effect.

2. In re Yamagata (Fig. 1E), has shown the structure with ***only one BJT 11 being created.*** It also should be noted that the n-well 3 is connected to the system high voltage Vcc. Also and, the source region 9 is grounded. Basically, ***Yamagata failed to disclose that the extended doped region 208 is adjacent to the source region 204a and the doped layer 206 in the same conductive type as recited in the present invention.*** If the N-well 3 is considered to be the doped layer 206 of the present invention, the N-well 3 is connected to the system high voltage Vcc but not the common voltage, such as the ground voltage.

The Office Action states that the first BJT transistor can be form by the source, drain and substrate in Yamagata. Applicant respectfully disagrees. Yamagata fails to specifically, disclose the ***first BJT transistor with the recited circuit connection*** due to the extended doped region 208 of the present invention.

For at least the foregoing reasons, independent claims 1 and 6 have patently defined over the prior art and should be allowed. For at least the same reasons, dependent claims 2-5 and 7-13 patently define over the prior art reference as well.

3. In re Steinhoff, Fig. 3B has disclosed only one BJT, which is composed by doped regions 350 and 352 with the substrate 338. However, Steinhoff failed to disclose the extended doped region 206 of the present invention. Steinhoff discloses the N-well 332, which connects the

N-buried layer 340 and the two doped regions 330 and 334 for the diode D2. It should be noted that, the N-buried layer 340 is coupled to the bonding pad and the protect circuit through the N-well 332 and the doped region 334 of the diode D2. Here, the doped region 334, the N-well 332 and the N-buried layer 340 are in the same conductive type and form a connection path. Clearly, ***the N-well 332 is in different operation and is not connecting the source 350 to the N-buried layer 340.*** In other words, ***Steinhoff failed to disclose the extended doped region 206 of the present invention.***

Therefore, even though the BJT 510 is created, it is still not in the same electric performance.

Further, the Office Action has noted that only the capacitor Cpn and the diode D1 are disclosed. It should be noted that the capacitor Cpn and the diode D1 are in parallel connection between the P-well 338 and the N-buried layer 340, which is further connected to the bonding pad 300 by the N-buried layer 340.

In other words, the capacitor Cpn and the diode D1 do not specifically disclose the second BJT of the present invention. In addition, the BJT 510 is not in the same circuit performance of the present invention, so as to form the two BJT's in connection at the drain region 204b.

For at least the foregoing reasons, independent claims 1 and 6 have patently defined over the prior art and should be allowed. For at least the same reasons, dependent claims 2-5 and 7-11 patently define over the prior art reference as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-13 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Oct. 20, 2005

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